3.5.2.1 Redundant Link

(Available only for an RMX, and only when a redundancy CPU is configured.) Choices:

- **Disabled:** The RMX is not used as a redundancy link. This RMX module is used just like the general purpose CMX module. All the remaining parameters on this tab are available.
- **Enabled:** The RMX is used as a redundancy link and cannot be used as a general purpose reflective memory module. All the remaining parameters on this tab are unavailable, and the Interrupt parameter is set to Disabled.

Default:

- Enabled when there are fewer than two RMX modules already set as Redundant Link in this target.
- Disabled when there are already two RMX modules set as Redundant Link in this target.

Note The Node ID, Redundant Transfer Mode, Rogue Master, and Network Memory Offset parameters are available for the RMX only when Redundant Link is set to Disabled.

3.5.2.2 Node ID

The unique number identifying this node in the reflective memory network.

Valid range: 0 through 255.

Default: 0.

3.5.2.3 Redundant Transfer Mode

Determines whether the packets are transferred once or twice.

Note All nodes on the network must use the same Redundant Transfer mode setting.

Choices:

- **Disabled:** Each packet is transferred once. This ensures the greatest effective network transfer rate, but increases the risk of data being dropped from the network.
- **Enabled:** Each packet is transferred twice. This greatly reduces the risk of data being dropped from the network, but also reduces the effective network transfer rate. For details refer to Chapter 3, the section, *Redundant Transfer Mode Operation*.

Default: Disabled.

3.5.2.4 Rogue Master

For details on Rogue Master operation, refer to Chapter 3, the section, *Rogue Packet Detection and Removal.*

Caution

Do not configure two nodes in the network as the same rogue master; otherwise, one of the two will erroneously remove packets before the data has been sent to all nodes in the ring.

Choices:

- **Disabled:** The module will not detect rogue packets.
- **Rogue Master 0 Enabled:** This Memory Xchange module is set as Rogue Master 0.
- **Rogue Master 1 Enabled:** This Memory Xchange module is set as Rogue Master 1.

Default: Disabled.

3.5.2.5 Network Memory Offset (MB)

Offset added to the address of network packets initiated by local bus writes to the reflective memory and subtracted from incoming network packets before applying them to the local reflective memory. For details on memory offset operation, refer to Chapter 3, the section, *Network Memory Offset*.

Valid range: 0 through 240 MB, in increments of 16 MB.

Default: 0.

3.5.2.6 Interrupt

(Read-only when the RMX Redundant Link parameter is set to Enabled.) Tells the system whether to expect a module interrupt from the Memory Xchange module. This parameter must be set to Enabled for the interrupt to trigger the execution of a block of logic.

Choices: Disabled, Enabled.

Default: Disabled.

Appendix C-Reflective Memory Module Status Bits

IC695CMX128, IC695RMX128, and IC695RMX228

In PACSystems Release 8.15 or later Module Status Bits are available for the IC695CMX128, IC695RMX128, and IC695RMX228 modules. These Module Status bits can be read using the BUS_READ_WORD function. If the function is successful, each bit returned will reflect the current state of the corresponding bit on the module faceplate, with a value of 0 being the equivalent of the LED being OFF, and a value of 1 being the equivalent of the LED being ON. This request will only work for reflective memory modules that are present and configured.

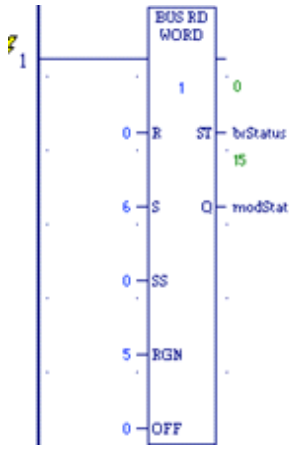
Instructions for Usage

To read this data use a BUS_READ_WORD function block:

```
LENGTH = 1

INPUTS:
 Rack = 0
 Slot = <actualSlot>
 Subslot = 0
 Region = 5
 Offset = 0

OUTPUTS:
 Status = BUS_RD_WORD execution status
 Q = Module status
```



If the ST output is 0, the data returned on the Q output of the BUS_READ_WORD block has the following format:

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Reserved				OWN DATA	SIG DE-TECT	LINK OK / CONFIG	OK

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Reserved							